KEYNOTE PRESENTATIONS

BIOGRAPHY

Professor Bailey is Director of the Computational Mechanics and Reliability Group at the University of Greenwich, UK. He has published over 300 papers on design, modelling, and simulation of electronics packaging technologies. He is a member of the Board of Governors for IEEE CPMT, Vice President for CPMT conferences, and is UK Chapter Chair for the IEEE CPMT and Reliability Societies. He is also a member of the technical working group on the new Heterogeneous Integration Roadmap focusing on co-design, modelling and simulation.

CO-SIMULATION AND MODELLING FOR HETEROGENEOUS INTEGRATION OF HIGH-TECH ELECTRONIC SYSTEMS

Professor Chris Bailey
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This presentation will detail the current status and future requirements of modelling and simulation tools in supporting chip, package, and board level co-design for advanced packaging (3D-IC's with TSV's, WLP, SiP, etc) of heterogeneous integrated systems. These tools will drive innovations across the die-package-system domains by optimizing electrical, thermal, mechanical and reliability performance for a diverse range of high-technology systems such as mobile devices, IoT, data centers, power conversion to name a few.

The presentation will provide a detailed overview on the different modelling methodologies for electrical, thermal and mechanical analysis as used today by the chip, package and board communities as well as the gaps that need to be addressed to ensure that cost effective co-design can be undertaken. This is particularly important as, for example, chip-package interactions are now becoming a major performance and reliability risk. Practical examples demonstrating current capabilities and areas for future research and development will be provided.